ENCAPSULATED DIE PACKAGE WITH IMPROVED PARASITIC AND THERMAL PERFORMANCE

Cross Reference to Related Applications

This application claims priority of U.S. Provisional Patent Application No. 60/271,940 filed on February 27, 2001 entitled "Encapsulated Die Package with Improved Parasitic and Thermal Performance", and the teachings are incorporated herein by reference.

Technical Field

The present invention relates to an enclosure for a semiconductor device and, more specifically, to an encapsulated molded common leadframe package. More specifically, the invention relates to such a package that limits unwanted parasitics and provides excellent thermal dissipation. The package is useful in three lead devices and two lead devices, including optoelectronic devices such as light emitting diodes.

Background of the Invention

In surface mount assembly, it is common to provide an enclosure or housing for encapsulating a semiconductor device. Currently, numerous package styles are available for surface mount assembly, such as the Standard Outline Transistor 23 (SOT 23), and the Standard Outline Diode 323 (SOD 323). These common leadframe injection molded packages have been used in the industry for

many years. However, such package styles suffer from various shortcomings including the existence of parasitics that limit the operating performance of the device past certain high frequencies. With such standard leadframe packages, the parasitics become inconsistent so that the distribution of parasitics varies from package to package. The result is that circuits and designs utilizing such packages tend to have inconsistency in performance with the results exaggerated as operating frequencies increase.

Moreover, standard package styles can suffer from very poor thermal paths between the surface upon which the semiconductor device is mounted and the thermal ground that provides attachment to the outside world, typically a circuit board. Accordingly, a need exists for a package style for a semiconductor device that provides good thermal properties and improved parasitic performance at higher operating frequencies.

Summary of the Invention

The present invention provides a semiconductor device package with improved thermal properties that limits unwanted parasitics and provides a more consistent distribution of parasitics from one device to another. Furthermore, the present invention provides a package with improved power handling capabilities or dissipation. Essentially, the package of the present invention is extremely compact and uses minimal length of bond wires between the terminals and the

attached device. The path length of the package is reduced so as to represent only some fraction of a wavelength relative to the terminals of the package. By reducing the length of the bond wires and selecting the appropriate dielectric constant of the encapsulant, the invention provides a package with a unique hexagonal structure that limits the effects of parasitics and provides good thermal dissipation. The package is useful with optoelectronic devices such as light emitting diodes where the encapsulant material is made of a substantially clear, including translucent, epoxy.

Brief Description of the Drawings

For a better understanding of the invention including its features, advantages and specific embodiments, reference is made to the following detailed description along with accompanying drawings in which:

Figure, 1 is a perspective view of a first embodiment of the semiconductor device package of the present invention;

Figure 2 is a top view of a first embodiment of the package, according to the invention, illustrating the arrangement of input/output and ground terminals;

Figure 3 is a side view of a first embodiment of the package of the present invention illustrating the connection of wire bonds from terminal to semiconductor die;

Figure 4 shows an alternate side view of a first embodiment of the package of the present invention;

Figures 5A, 5B and 5C illustrate close-up views of a first embodiment of the package of the present invention with dimensions noted thereon;

Figures 6A, 6B and 6C illustrate close-up views of a first embodiment of the package of the present invention with dimensions noted; and

Figures 7A, 7B, 7C and 7D illustrate close up views of the package according to a second embodiment of the package of the present invention with dimensions noted.

Figures 8A, 8B and 8C illustrate close up views of the package according to a third embodiment of the package of the present invention with dimensions noted.

Figures 9A, 9B and 9C illustrate views of the package according to the second and third embodiments of the package of the present invention with dimensions noted.

References in the detailed description correspond to like references in the figures unless otherwise noted.

Detailed Description of Embodiments

While the making and using of various embodiments of the present invention are discussed in detail below, it should be appreciated that the present

invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts.

The present invention provides a package suitable for use in housing a semiconductor device, including as part of an integrated circuit, in a surface mount assembly. Figure 1 illustrates a first embodiment of the package 10 as including an encapsulant material 12 with input terminal 14, output terminal 16 and ground terminal 18. As shown in Figures 2 and 3, a first embodiment of the package 10 is arranged so that bond wires 20 and 22 extend from terminals 14 and 16, respectively, and are attached to a semiconductor device 30 attached to an upper surface of the ground terminal 18.

The bond wires are maintained at a minimal length and the dielectric constant of the encapsulant material 12 is selected such that the performance of the device 10 is predictable, therefore enhancing the ability of the device 10 to minimize unwanted parasitics as the frequency of operation of signals coupled to the input terminal 14 increases. This enhances the consistency of the package 10 from one device to another. As illustrated in Figure 1, the encapsulant material 12 has taken the form of a hexagonal structure that allows the use of the ground terminal 18 as a shunt comprising the surface where the device 30 is mounted. This surface wraps around the ground terminal 18 essentially at right angles and reaches down to the bottom surface, greatly enhancing the thermal path to ground.

This results in overall less thermal capacitance and considerably less thermal resistance.

As is well known in the arts, the power handling capabilities of a semiconductor package depend on how much heat can be dissipated by the device. Too much heat can interfere with the operation of the semiconductor device 30, and as such, heat dissipation is a property of the package 10 that must be controlled accurately. As shown in Figures 2, 5A and 6A, a first embodiment of the package 10 includes conductive leadframe portions in the form of input terminal 14 and output terminal 16 such that power is applied to one side (the input terminal 14) to the device 30 and is output on an opposite side (the output terminal 16). Running approximately orthogonal to the input 14 and output 16 terminals is the ground terminal 18 which provides a shunt extending around the terminal 18, such that the electrical properties of the device 10 are controlled.

Since the bond wires 20 and 22 are kept short, package performance from one device to another is more consistent compared to SOT 23 and SOD 323 type packages. Also, since the parasitic capacitance is a function of dielectric constant of the encapsulant material 12, its performance is further improved and more predictable. The input and output terminals 14 the 16 are not parallel to each other, therefore avoiding parallel conductive surfaces which could create unwanted parasitics. Also, the input 14 and output 16 terminals have a rounded

portion 24 and 26 which allow the length of the bond wires 20, 22 to be relatively short and further improves the performance of the device 10.

Figures 5A, 5B, 5C, 6A, 6B and 6C illustrate dimensions of the device, according to the first embodiment. It should be understood that changes to these dimensions can and will occur to those of ordinary skill in the art.

Therefore, the package 10 includes a unique orthogonal leadframe configuration which allows direct dissipation shunting to thermal ground while providing low inductance electrical connections to die which supports device functionality. In one embodiment, the device 10 operates with good results up to 10 gigahertz. Furthermore, the device 10 provides controlled dielectric constant encapsulant 12 which results in improved unit-to-unit and run-to-run package parasitic consistency. This results in improved RF performance consistency. Moreover, the package mounting footprints allows for visual confirmation of solder fillet, unlike flip-chip package designs which result in a blind solder joint. The package 10 allows for single or dual two-terminal devices (as noted below), three-terminal devices, as. well as gain stages. The unusually thick leadframe material allows a dovetail type of side edge so the epoxy can lock on the leads on only three sides. This is accomplished with unique half edge features which allow a mold with one side of the leadframe remaining completely bare copper. Because of the uniqueness of the assembly process, the package 10 allows the thermal path

of the die to be outstanding. The full metal bottom allows the heat to transfer directly to a printed circuit board. Leadframe design allows wire bond wires 20, 22 to be extremely short for the package size.

Figures 7A, 7B and 7C illustrate a second embodiment of the present invention for use with two lead devices, including optoelectronic devices such as light emitting diodes. As seen in Figure 7A, if the two lead device is a light emitting diode, then encapsulant material 12 is made of a substantially clear epoxy, with anode 71 and cathode 72. As illustrated therein, the substantially clear encapsulant material 12 has taken the form of a hexagonal structure. The surface of the encapsulant wraps around the anode 71 and cathode 72 and reaches down to the bottom surface, greatly enhancing the thermal path to ground. Further, as can be seen in Figure 7B, the anode 71 and the cathode 72 are positioned opposite to each other, with the cathode 72 further comprising a portion of a conductive lead-frame. The anode 71 has a shaped end surface operable to minimize parasitic capacitance. Alternatively, the cathode 72 could comprise metallization as the means of coupling the cathode 72 to the semiconductor die 30. As seen in Figure 7B, a bond wire 22 couples the anode 71 to the semiconductor die 30. The bond wire 22 could have a length comprising a fraction of the wavelength for which frequency the semiconductor device 70 is designed. The packaged semiconductor device 10 as seen in Figure 7A is adapted

for use in an integrated circuit and is advantageously suited for use in a surface mount assembly. This configuration of the semiconductor device 10 as seen in Figure 7A results in overall less thermal capacitance and considerably less thermal resistance.

Figures 8A, 8B and 8C illustrate a third embodiment of the present invention also for use with two lead devices, including optoelectronic devices such as light emitting diodes. As seen in Figure 8A, encapsulant material 12 is also made of a substantially clear epoxy, with anode 71 and cathode 72. As distinguished from Figure 7B, in Figure 8B, the anode 71 comprises a portion of a conductive lead-frame. The cathode 72 has a shaped end surface operable to minimize parasitic capacitance. Alternatively, the anode 71 could comprise metallization as the means of coupling the anode 71 to the semiconductor die 30. As seen in Figure 8B, a bond wire 22 couples the cathode 72 to the semiconductor die 30. The bond wire 22 could have a length comprising a fraction of the wavelength for which frequency the semiconductor device is designed. The packaged semiconductor device 10 as seen in Figure 8A can be adapted for use in an integrated circuit and for use in a surface mount assembly. This configuration of the semiconductor device 10 as seen in Figure 8A results in overall less thermal capacitance and considerably less thermal resistance.

Figures 7B, 7C and 7D illustrate representative dimensions of the device, according to the second embodiment of the present invention. Figures 8A, 8B and 8C illustrate representative dimensions of the device, according to the third embodiment of the present invention. Figures 9A, 9B and 9C illustrate representative dimensions of the device, according to the second and third embodiments of the present invention. It should be understood that changes to these dimensions can and will occur to those of ordinary skill in the art.

While the invention has been described with regard to specific and illustrative embodiments, this description and the following claims are not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments as well as other embodiments of the invention will become apparent to persons skilled in the art upon reference to the description and is intended that such variations be encompassed and included within the meaning and scope of the following claims.